

ECE 453 Software Practicum

Fall 2004

Objective

In this course students will work in three-person teams to construct a simulation of an embedded processor, along with accompanying development tools. Specifications will be developed throughout the semester. The final project will consist of (at least) three parts: an instruction-level simulator, a chip pin-level simulator, and a hardware development board. The software pieces will be designed to plug into a larger development environment, in which a user can select processor(s) and other parts to test designs. The gcc compiler will be used to cross-compile code to all target processors. Compiled code should be able to execute on the simulations as well as on the development board (the real chip).

Two graduate students will supervise this project. Krishna Sagiraju will create the main development environment, and lead the integration of chip simulations into that environment. Peter Rickenbach will create a unified development board and lead the hardware integration.

Meetings will be held weekly (Tuesdays) to brainstorm solutions, refine specifications and interfaces, and report progress. Attendance at these sessions is required.

Text

There is no text. However, each team will be required to purchase one or more chips for development. Teams also have the option of purchasing existing development tools in order to learn how they work.

Professor

Dr. Adam Hoover
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656-3377
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office hours walk-in anytime, or by appointment

Lab

Riggs 215/217 is the primary lab for this course. Teams may elect to do development work elsewhere, but ultimately everything must operate in this lab. The workstations in that lab are running linux. Everything for this project is expected to run under linux using the open source philosophy.

Grading

There will be only one grade, given at the end of the semester. Final *team* grades will be determined via ranking. The best team(s) will get an A, followed by appropriate grades for the other teams. The measure of a team's success will be the functioning, accuracy, and speed (in that order) of the simulations, and the ease of transition to the real chip.

Final *individual* grades will be adjusted based upon the instructor's evaluation of participation and solicited feedback from the teams. This feedback will be gathered anonymously at the end of the semester, when each individual will have the chance to characterize their teammates' contributions and performance.