

ECE 201 Lab - Four-bit Adder/Subtractor with Decimal Output

Objectives

To familiarize students with MSI technology, specifically adders. The student should also become familiar with 1's complement arithmetic.

Background

In the last experiment we built a pair of adders and used them to add 2-bit numbers. In this lab we will use an MSI chip containing four full adders to add and subtract 4-bit signed numbers using 1's complement arithmetic. All of the chips used thus far have been SSI (Small Scale Integration) chips which consist of single gates. MSI (Medium Scale Integration) chips combine dozens of gates into a single function on a chip, in this case a 4-bit full adder, the 7483. LSI (Large Scale Integration) and VLSI (Very Large Scale Integration) combine hundreds or thousands of gates into very complex devices on a single chip. Microprocessors and related components fit into these categories.

Remember that by using 1's complement arithmetic we can both add and subtract with the same circuitry. The problem remains of how to complement a number so that subtraction can be performed.

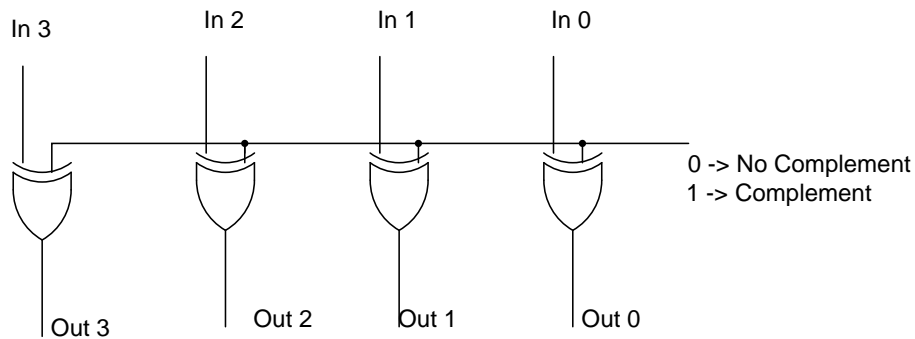
Procedure

Part I

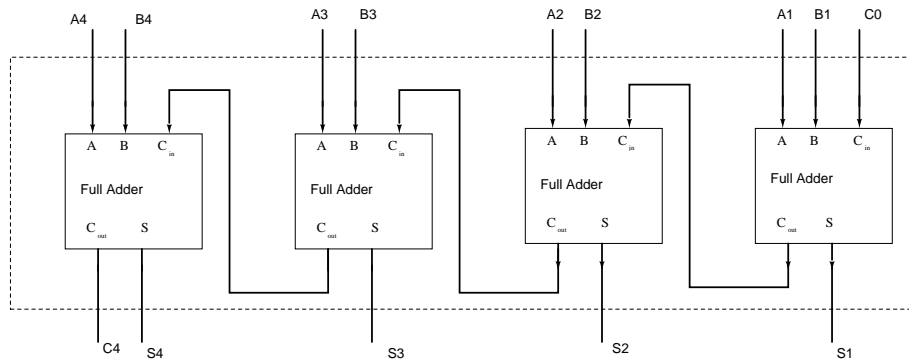
Let's look at an EXOR gate. Note that if one input is 0, the output equals the other input. On the other hand, if one input is 1, then the output equals the complement of the other input.



We can thus use EXOR gates to perform a one's complement on command.

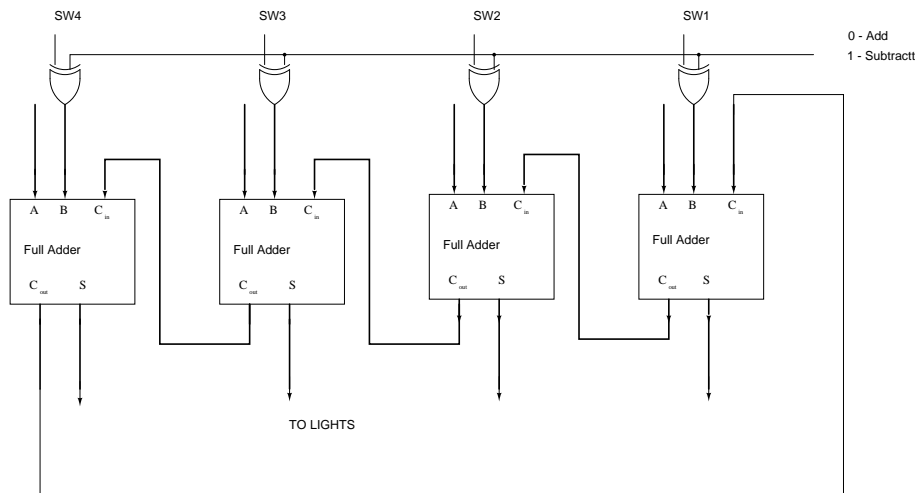


In block diagram form, the 7483 appears as shown:



Note that the carries are already inter-connected within the chip (right most carry in and left most carry out are available for cascading or other uses). The A's and B's are the inputs and the R's are the outputs.

Label the pin numbers on the following circuit, construct it, and verify that it both adds and subtracts A and B. Caution: Check pin #'s for power and ground.



Since we have only 4 switches, we use these for A and will simply plug the B's into either +5V or GRD to produce B. E. G. B4 = GND, B3 = GND, B2 = +5V, B1 = +5V would be the number 3. What happens if we add 0011 and 0111? Is the result correct? Why or why not?

Why was C4 connected to C0?

NOTE: Be sure both chips are at one end of the breadboard to facilitate the further expansion of the circuit.

Part 2

It would be handy if we could display our results in a more easily readable form. Using another EXOR package, a seven-segment display, a few resistors (to limit current so the seven-segment display won't smoke) and a decoder to convert BCD to seven-segment format (contains decoders for each segment similar to the single "b"-segment decoder of Lab 2) this goal may be achieved by means of the following circuit. (Construct and test.)

