

ECE 201 Lab - Sequential Design Design of a three bit counter

Objectives

This lab should illustrate the design of synchronous circuits, as well as demonstrate design restrictions. The student should also experience relief, since this is the last lab.

Procedure

This lab requires the normal prelab report, with a complete schematic, and an explanation of the design process. This should include state transition tables; K-Maps, and Boolean reductions for every appropriate variable. Answer all questions posed in the lab.

Assume that you have nearly completed a stupendous project designed to control the universe. All you lack is a simple 3-bit up/down counter. You look in the parts bin and see almost nothing, and certainly not a counter. It is Sunday, thus you can't rush down to Radio Shack and buy one. You are desperate! What if a giant meteorite were to smash into your workshop and obliterate your creation only hours before you gained control (and thus could prevent the meteorite from doing so)?

Looking in your parts bin again you find the following parts:

- 1 - 7476 Dual JK f/f
- 1 - 74175 Quad D f/f

Several of each of the following:

- 7408 - Quad 2-input AND
- 7432 - Quad 2-input OR
- 7486 - Quad 2-input XOR

Next you realize that the only thing remaining for you to construct the counter on is one of those old dilapidated Digi-Designer boxes which your school had finally thrown away, thus you are limited to five chips.

It is immediately obvious that the 7476 is insufficient since you need 3 f/f, thus you start by choosing the 7415 which contains 4 f/f. Next you do a quick design, and using c as the control bit variable ($c=0$) means count up and vice versa) and $Q_3Q_2Q_1$ as the counter bits you obtain the following equations for the 3 D inputs:

$$D3 = cQ_3'Q_2'Q_1' + c'Q_3'Q_2Q_1 + c'Q_3Q_2' + cQ_3Q_1 + Q_3Q_2Q_1'$$

$$D2 = cQ_2'Q_1' + cQ_2Q_1 + c'Q_2'Q_1 + c'Q_2Q_1'$$

$$D1 = Q_1'$$

With only 2 input AND and OR gates, the decoding for D3 alone would require 4 packages, thus the Digi-Designer is not large enough. Leaving that for the moment, you move on to D2. This looks bad superficially but after a moment's reflection you realize that can be implemented with 2 2-input XOR gates. D1 must have Q_1' , but this is available on the 74175. Well, 2 out of 3 implemented and less than 2 full chips used isn't bad for a start.

If you could implement the remaining bit with 3 or fewer chips (plus 2 XOR gates) the universe is at your command! You next try using a JK f/f for bit 3. (You decide trying to figure out how to use some XOR's to implement D3 would take too long and might not work anyway.) As it turns out, the J and K inputs for Q_3 can be realized using one 7408 and one OR gate. You spontaneously burst into fiendish maniacal laughter.

Anyway, let's finish the explanation of the gizmo so you can be done with 201 Lab. (Thunderous applause.) Determine the appropriate circuitry for J and K, and connect the whole mess using a switch for the control bit. In addition, connect one of the pulsers to the clear inputs of the 7476 and the 74175 to allow presetting of the counter to 000. (This should be the pulser pin that goes low when the button is pressed.) Note that the preset pin of the 7476 MUST be tied to +5V. Use 3 lights for the output. (Which bit goes to the left most light?) Use the clock at 1 Hz to clock the circuit.

HINTS

- Make out the complete state transition table to get J & K. This is not absolutely necessary but may avoid confusion and errors. Compare the equations for J and K!
- If you don't immediately see how to implement D2 with 2 XOR's, factor out the c and c' terms, then fiddle with the terms being AND'ed with c and c' until you recognize the XOR.
- Use an extra XOR to invert c. (Remember how to do that?)

Verify that the circuit counts up if c=0 and down if c=1. Also verify that the pulser clears the counter.

Note: The clock of the 74175 must be inverted relative to that of the 7476. Either use the complimentary clock outputs on the Digi-Designer or invert the clock with an XOR.

WARNING

Watch the power connections on the 7476. If you hook up pin 13 to +5V and pin 5 to GRD, You will destroy the chip! (I know - I learned the hard way.)

QUESTION

Is it possible to implement D3 within the stated limitations? If so, how?