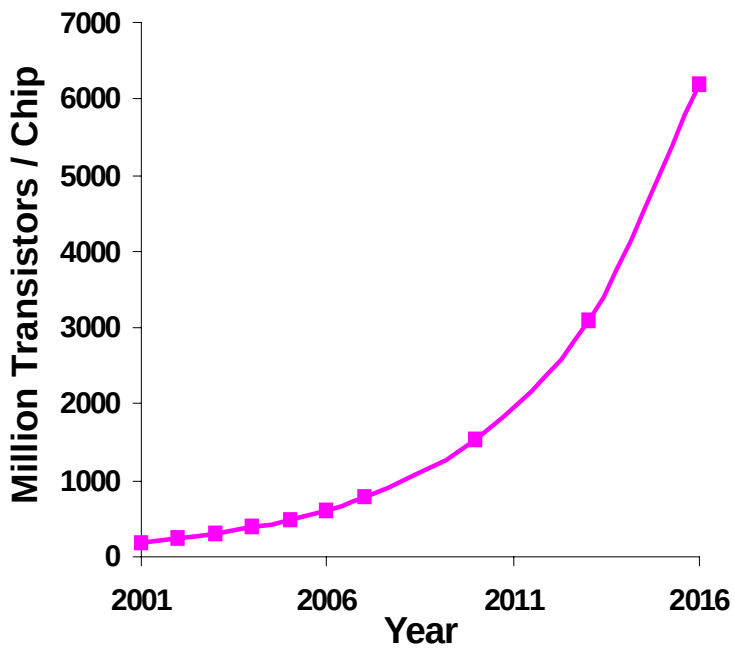
Research Interests

- Processor Performance Modeling
- Processor Power Reduction

Processor Design

Processor design time is increasing

- Design time ∝ number of transistors
- Transistors per chip* increasing
- Greater processor complexity is making design time crucial

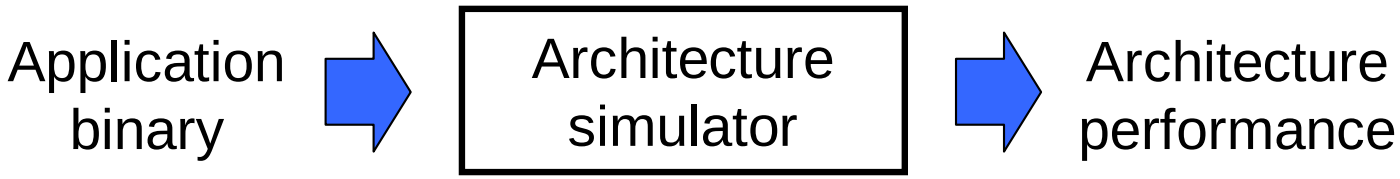


*International Technology Roadmap for Semiconductors, 2001 Edition

Current Design Methods

Design with cycle-accurate simulators

- Detailed
- Accurate
- Slow
- Time needed to build (weeks)
- Do not consider semiconductor technology



Simulation Time

Long program lengths:

- Billions of instructions
- At least 4.5 hours on UltraSPARC II

Arch 1	cc	compress	go	ijpeg	li	m88ksim	perl	vortex

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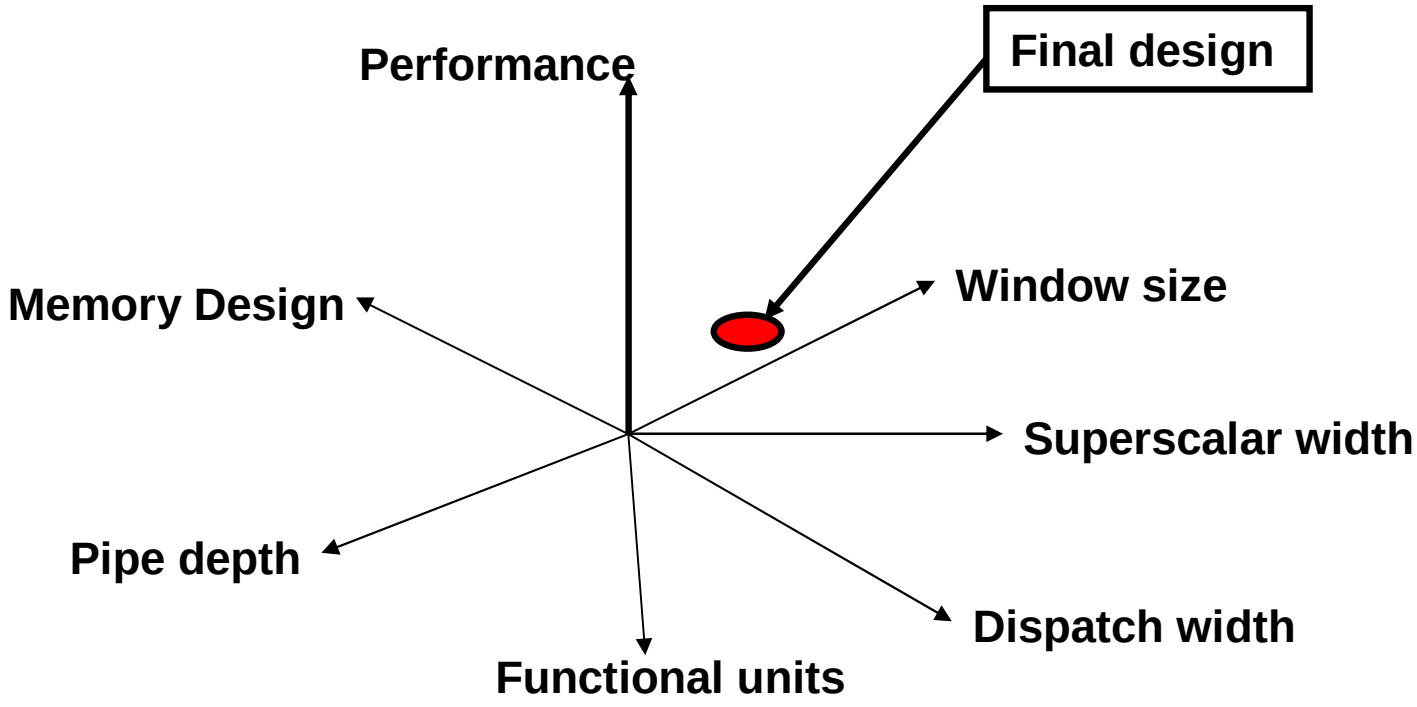
Arch 2	cc	compress	go	ijpeg	li	m88ksim	perl	vortex
Arch 3	cc	compress	go	ijpeg	li	m88ksim	perl	vortex
Arch 4	cc	compress	go	ijpeg	li	m88ksim	perl	vortex
⋮		⋮		⋮			⋮	
Arch 1999	cc	compress	go	ijpeg	li	m88ksim	perl	vortex
Arch 2000	cc	compress	go	ijpeg	li	m88ksim	perl	vortex

2000 configurations take 8.2 years to simulate!

Design Complexity



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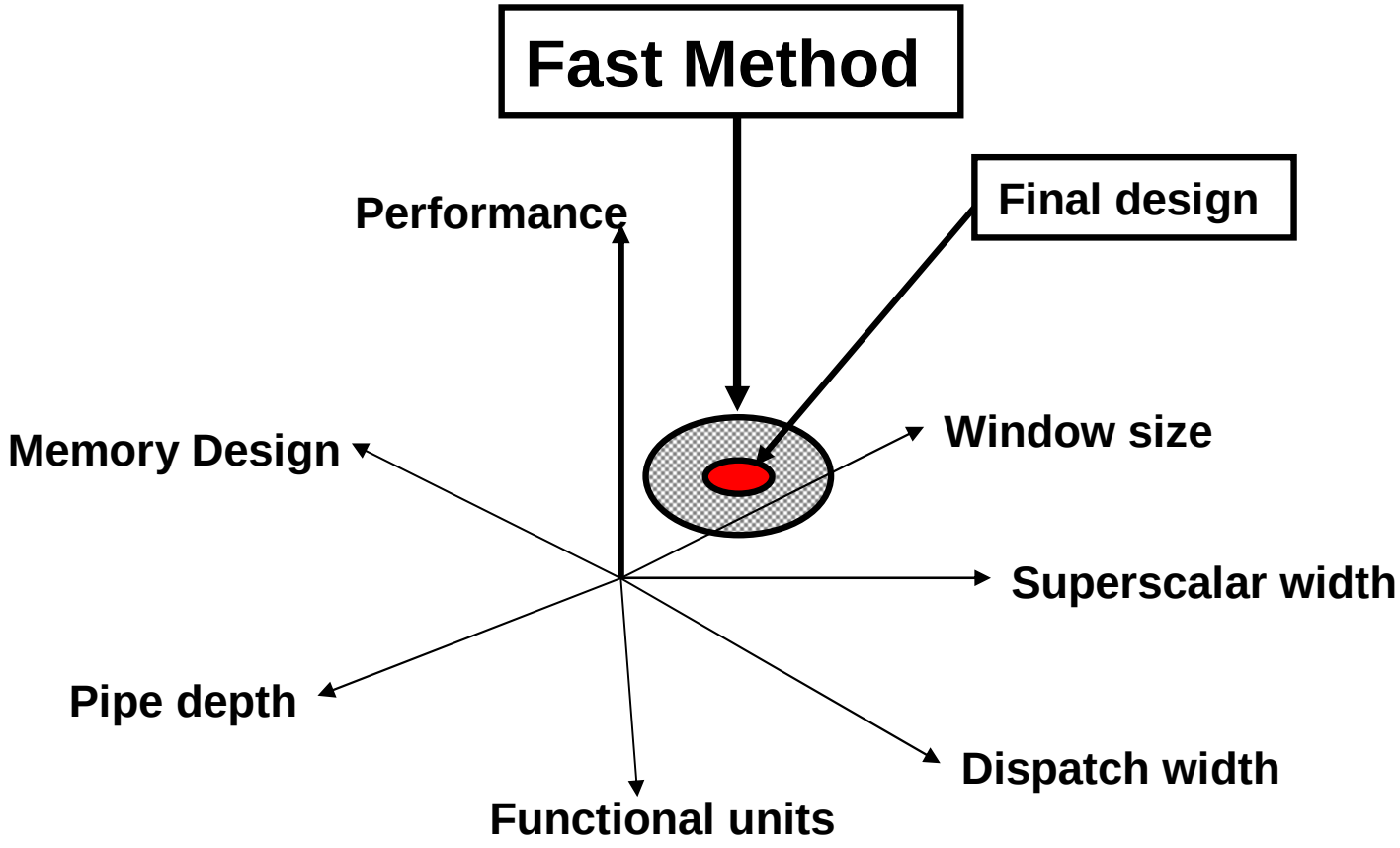
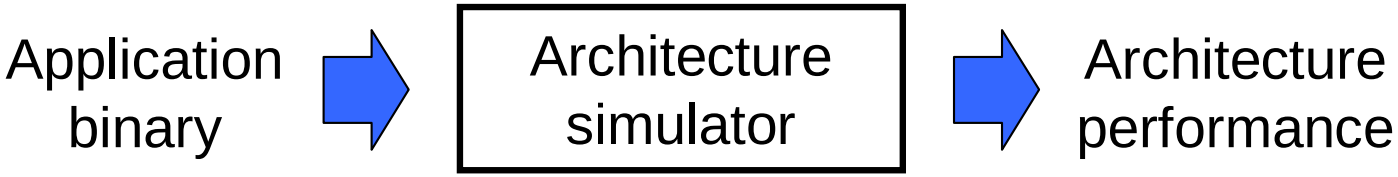


Faster Modeling Methods



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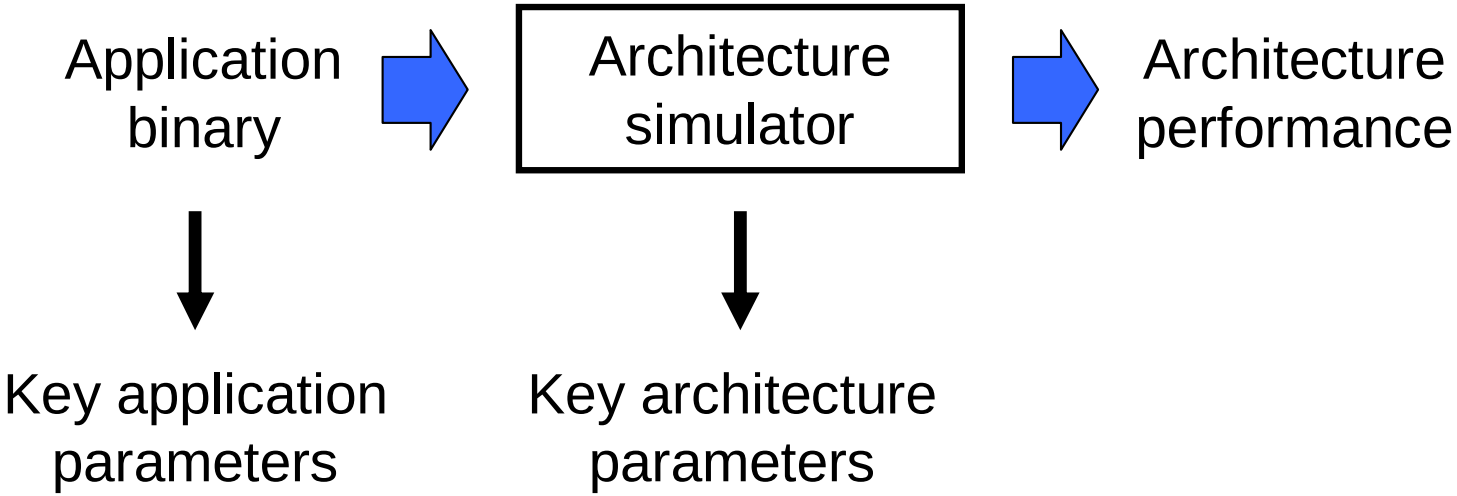

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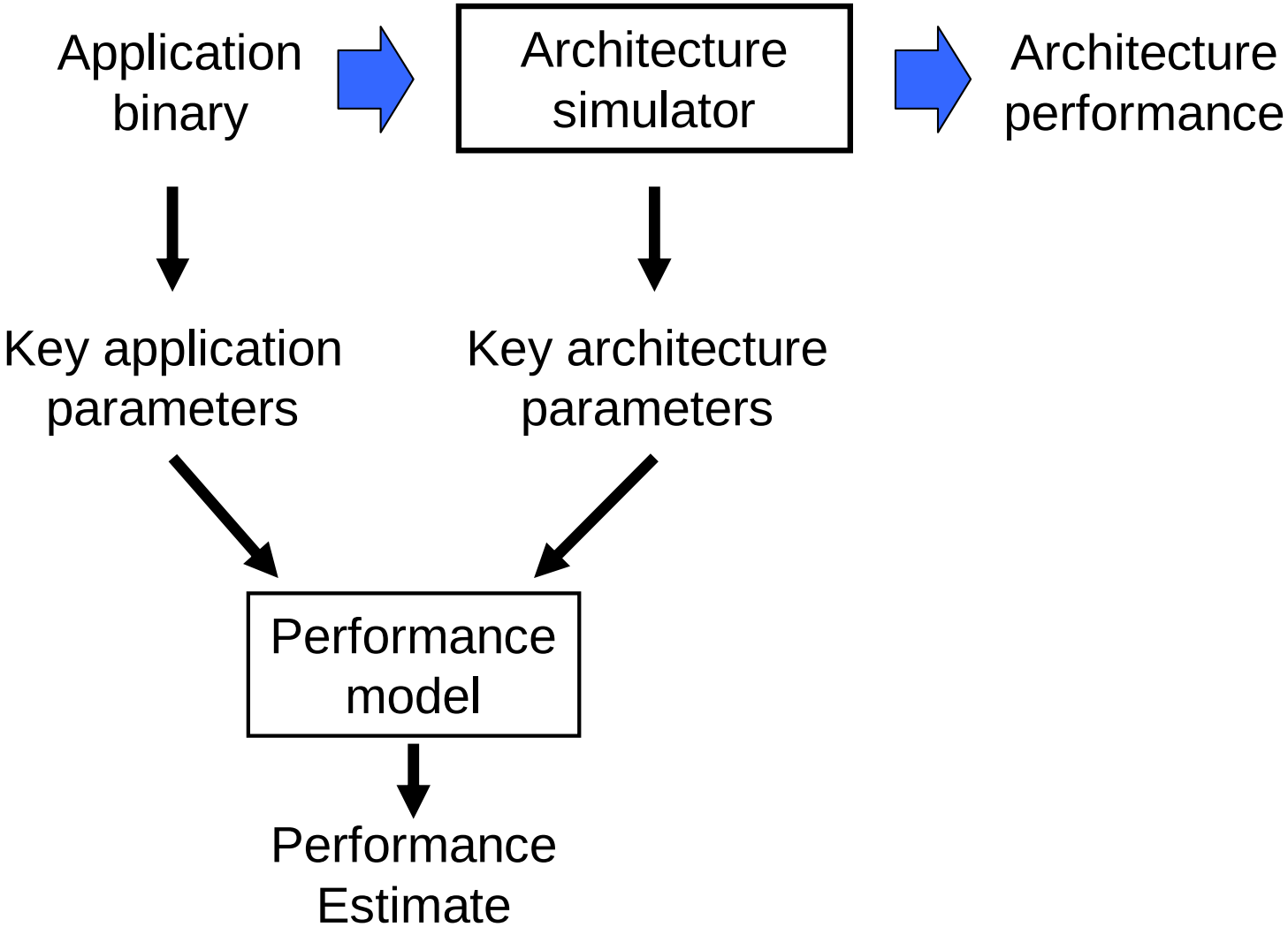

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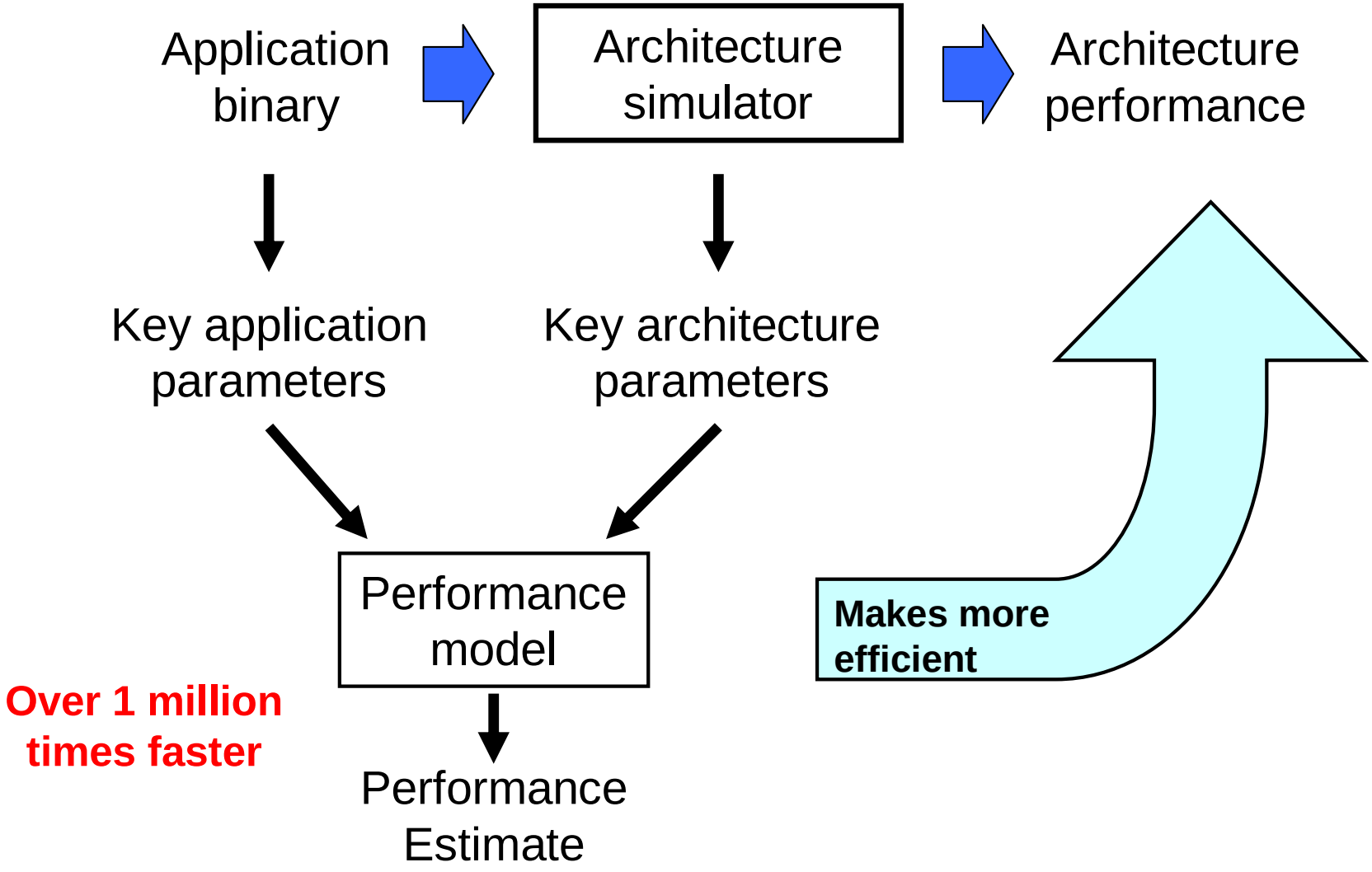
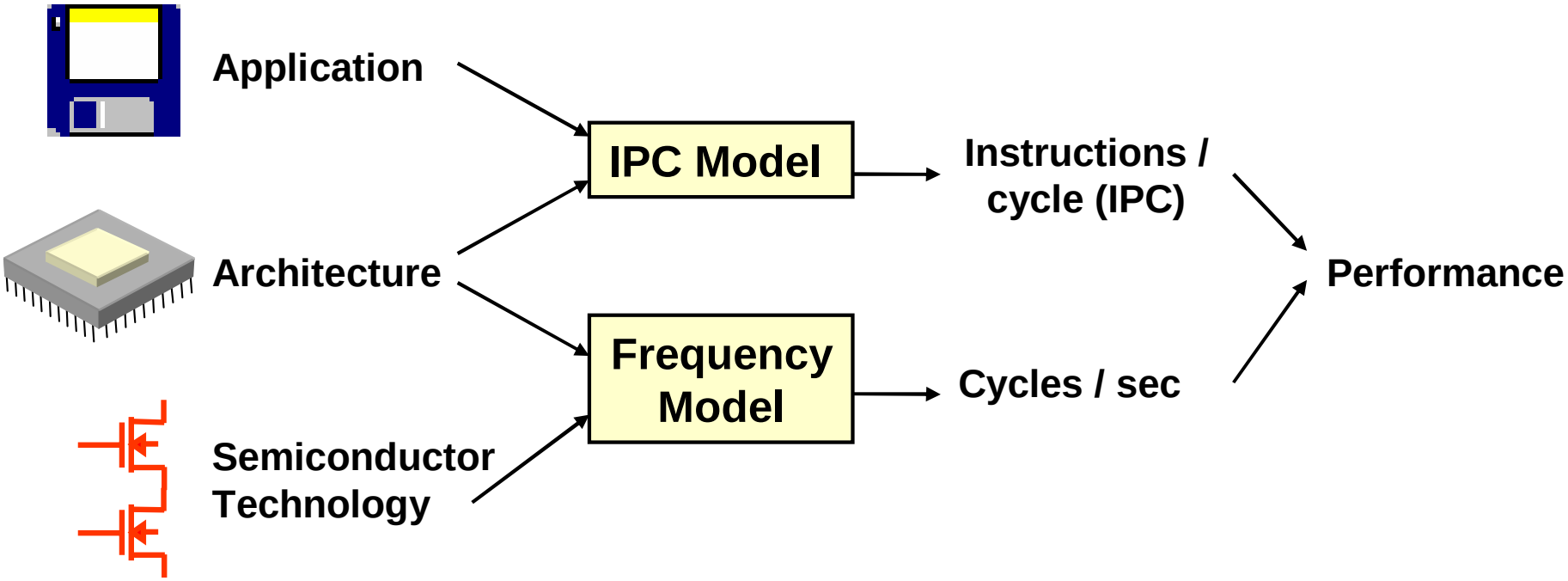
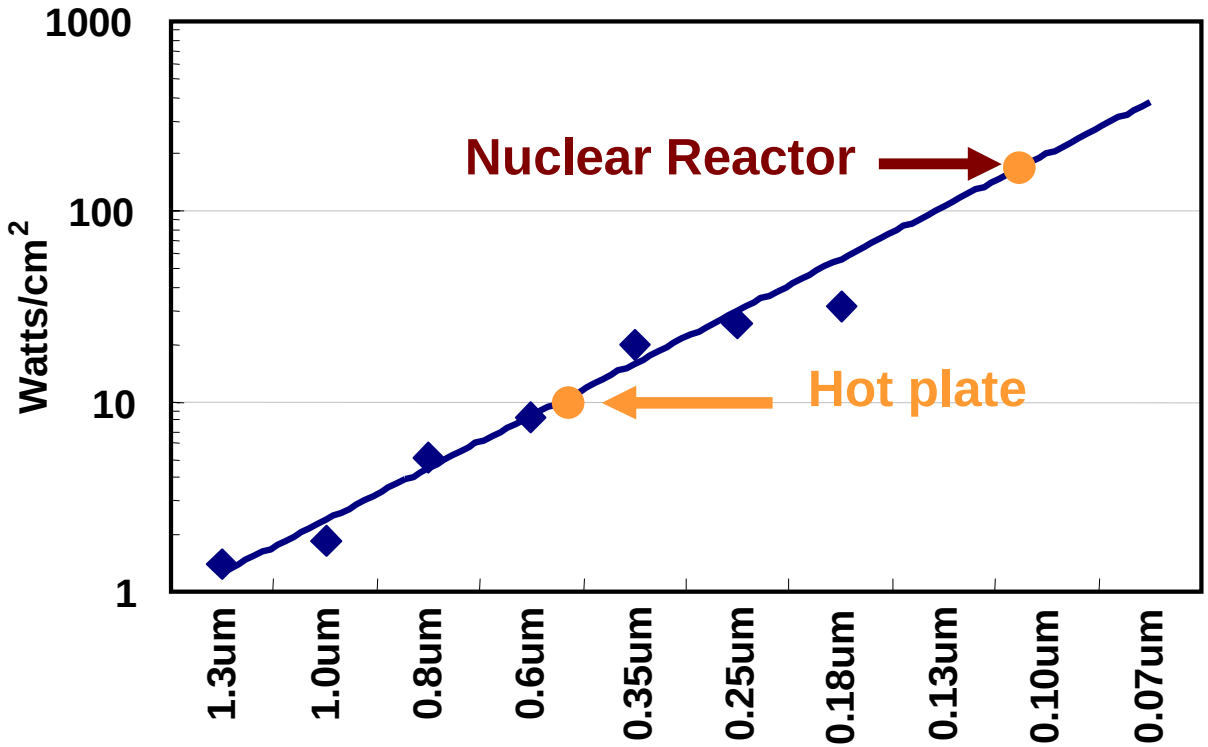


Analytical Model Components

$$\text{Instructions / time} = \underbrace{\text{instructions / cycle}}_{\text{IPC}} \times \underbrace{\text{cycles / time}}_{\text{Frequency}}$$



Processor Power Consumption

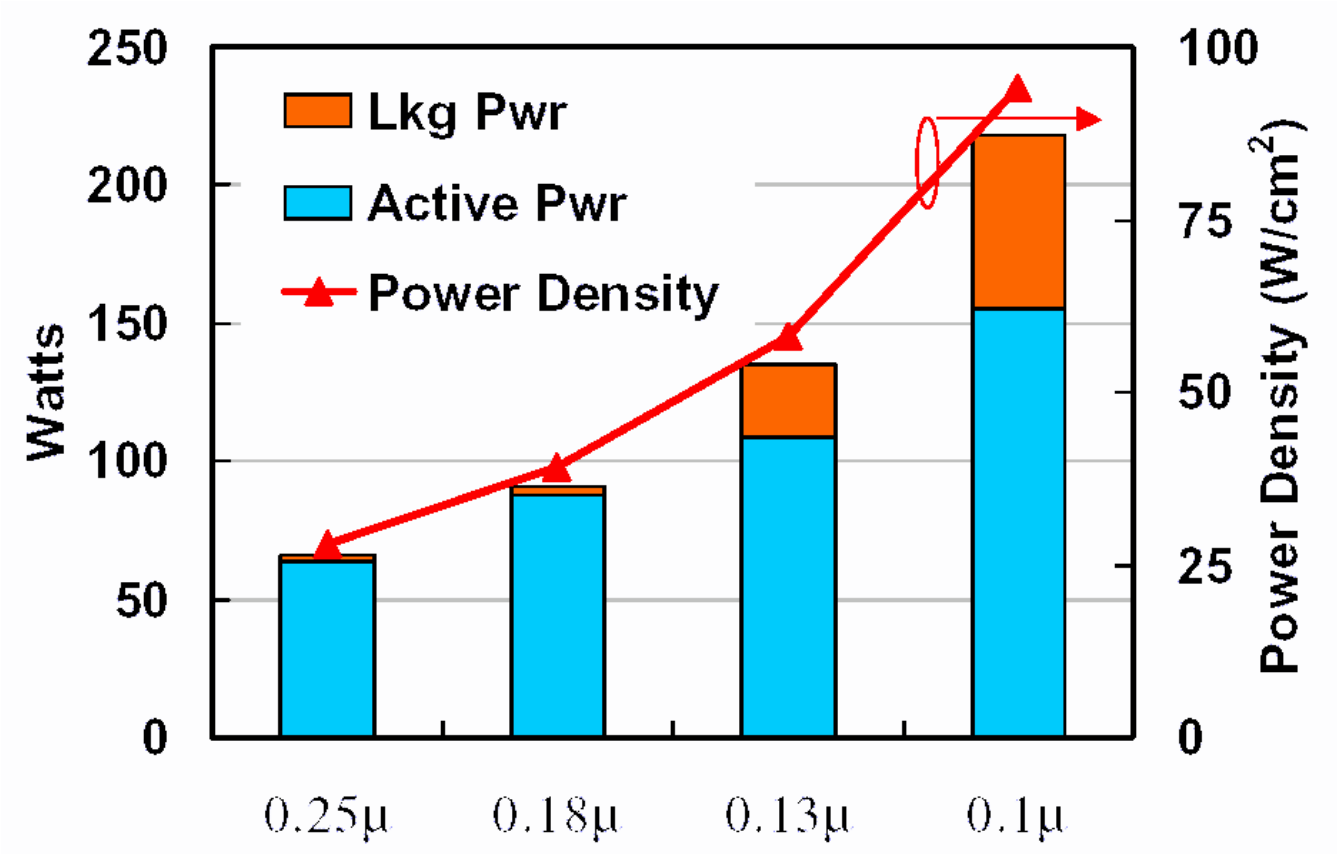


Source: Intel
S. Borkar

Surpassed hot-plate power density in 0.6um

Not too long to reach nuclear reactor

Types of Power Dissipation



Source: Intel
F. Pollock

Power of two main types: active and static (leakage)
Static power is rapidly exceeding active power

Static Power Reduction

- Controlling static power:
  - Device/circuit techniques rapidly running out of steam
  - Turn off units
  - Reduce unit speeds

- Hinders performance
- Architecture problem

Architecture Solutions

- Power gating to functional units
  - Monitor instruction usage to turn off units
- Drowsy caches
  - Put cache lines in low power state
- Need fast performance modeling of techniques